REMARKS

The Office Action mailed March 28, 2001, has been received and reviewed. Claims 1 through 4 are currently pending in the application. Claims 1 through 4 stand rejected. Claims 3 and 4 have been amended herein. Applicants respectfully request reconsideration of the application in view of the arguments set forth below.

Double Patenting Rejection Based on U.S. Patent No. 6,048,744

Claim 4 stands rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, and 5 of U.S. Patent No. 6,048,744. In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 CFR §1.321 (b) and (c). Applicants' filing of the terminal disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejections. Attached is the terminal disclaimer and accompanying fee.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,714,792 to Przano

Claims 1 through 3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Przano (U.S. Patent No. 5,714,792). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner cites Przano as teaching all of the elements set forth in claims 1 through 3. In support of the position that Przano teaches an alignment feature the Examiner states the following in a footnote:

> Examiner has interpreted an alignment feature to include a tie bar and a die support bar. This interpretation is based upon the applicant's definition of an alignment feature (see specification at 9) in which the "alignment portion 422 includes a tie bar 424 and also other parts of the lead frame 420 which provide internal support to the integrated circuit package." (Office Action, FN 1).

Applicants respectfully disagree with Examiner's interpretation of the claim language "an alignment feature," and further submit that, contrary to the Examiner's assertion, the specification fails to support the above stated interpretation.

Applicants submit that, on its face, an "alignment feature" refers to an element or structure, which allows for the proper positioning or adjustment of various components in relation to each other. In contradistinction, a tie bar or die support bar are members of a lead frame known in the art for supporting a semiconductor die during packaging. An alignment feature and a support member are elements, which serve vastly different purposes, and the existence of one does not indicate the existence of the other.

With respect to the Examiner's interpretation of the specification, it is noted that the passage relied on is set forth in explanation the embodiment depicted in FIG. 4. Referring to FIG. 4 and to the related portions of the specification, it is stated that an "integrated circuit 400 is provided with a lead frame 420 having alignment *features* 410." (Specification, page 9, lines 5-6, emphasis added). Furthermore, it is stated that the "lead frame 420 has leads 430 and an alignment *portion* 422." (*Id.*, line 7, emphasis added). It is noted that the alignment *portion* is part of the alignment *feature* not the entirety thereof. In further describing the embodiment of FIG. 4 it is stated that the "alignment *portion* 422 *includes* a tie bar 424 and also other parts of the lead frame 420 which provide internal support to the integrated circuit package." (*Id.*, lines 7-9, emphasis added). Thus, the tie bar 422 does not even form the entirety of the alignment *portion*. In conjunction with the alignment *portion* (and as part of the alignment *feature*) the "lead frame has cut outs 450 integral therewith, disposed within the alignment portion 422." (*Id.*, lines 11-12). It is apparent from FIG. 4 that without the alignment cutouts 450, the tie bar would serve no other purpose than to provide internal support to the integrated circuit package. Thus, the alignment *feature* requires more than just the tie bar, which is referred to in the specification as *part* of the alignment *portion*.

Therefore, Applicants submit that "an alignment feature" as recited in the presently claimed invention cannot be interpreted simply as a tie bar or die support bar. Such an interpretation is not supported by common usage of the term, nor is such an interpretation supported by the specification.

In view of the foregoing, Przano clearly fails to teach all of the elements of the presently claimed invention.

With respect to claim 1, Przano fails to teach a method of forming an integrated circuit package which includes the formation of a lead frame having a plurality of conductors and *at least one alignment feature electrically isolated from the plurality conductors*. While the Examiner relies on the existence of tie bars as alignment features, Przano never mentions the

incorporation of any other element or structure with the tie bars for the purpose of forming an alignment feature. As such, claim 1 is clearly allowable over Przano.

Applicants submit that claim 2 is allowable at least by reason of its dependency from claim 1, which is allowable. Furthermore, claim 2 recites that the method of forming an integrated circuit package additionally include removing the at least one alignment feature. The Examiner refers to col. 4, lines 51-57 of Przano for the teaching of such subject matter. However, Przano actually teaches that the "*tie bars* 20 are no longer joined to the rails 12 but are instead severed and flush with an edge of the package body." (Col. 4, lines 52-53, emphasis added). Having no alignment feature in the first place, it is impossible that Przano can teach the removal of an alignment feature. Rather, Przano simply teaches the trimming of tie bars.

Furthermore, even if Examiner's interpretation regarding the equivalency of a tie bar and an alignment feature was accepted (which Applicants maintain their traversal of such interpretation), Przano does not teach the *removal* of the tie bar, but rather the *severing* and *trimming* of the tie bar such that it did not extend beyond the edge of the package body.

With respect to claim 3, Przano fails to teach a method of forming an integrated circuit package, which includes providing a plurality of conductors *and at least one alignment feature*. Nor does Przano teach *substantially encompassing the at least one alignment feature with an insulating material*. The Examiner relies on col. 4, lines 47-50 of Przano as teaching the encapsulating of an alignment feature. However, as set forth above, Przano fails to teach the formation of alignment feature, thus it fails to teach the encapsulation of an alignment feature. Thus, Przano clearly fails to anticipate the presently claimed invention as set forth in claim 3.

ENTRY OF AMENDMENTS

The amendments to claims 3 and 4 above should be entered by the Examiner because the amendment are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 4 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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BBJ/ps:blh
Date: June 25, 2001
Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (Amended) A method of forming an integrated circuit package, the method comprising:

providing a plurality of conductors and at least one alignment feature;

coupling at least some of the plurality of conductors to a semiconductor die; and

encompassing the semiconductor die, [the at least one alignment feature, and] a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material.

4. (Twice Amended) A method of forming and testing an integrated circuit package, the method comprising:

providing a plurality of conductors and at least one alignment feature;

electrically coupling at least some of the plurality of conductors to a semiconductor die;

encompassing the semiconductor die, [the at least one alignment feature, and] a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material;

coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and

testing the integrated circuit package through at least some of the electrically coupled conductors.